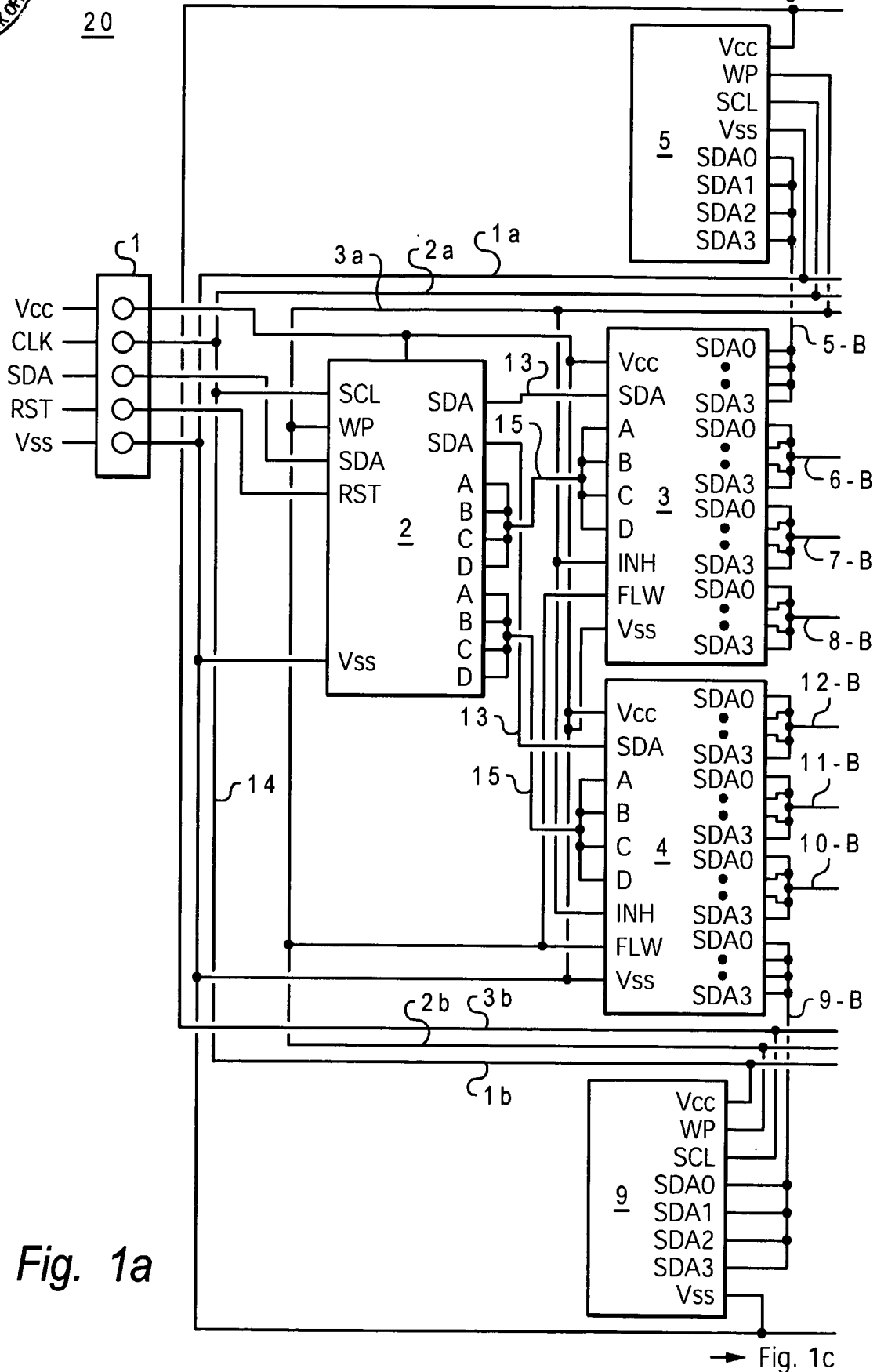


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→ Fig. 1b





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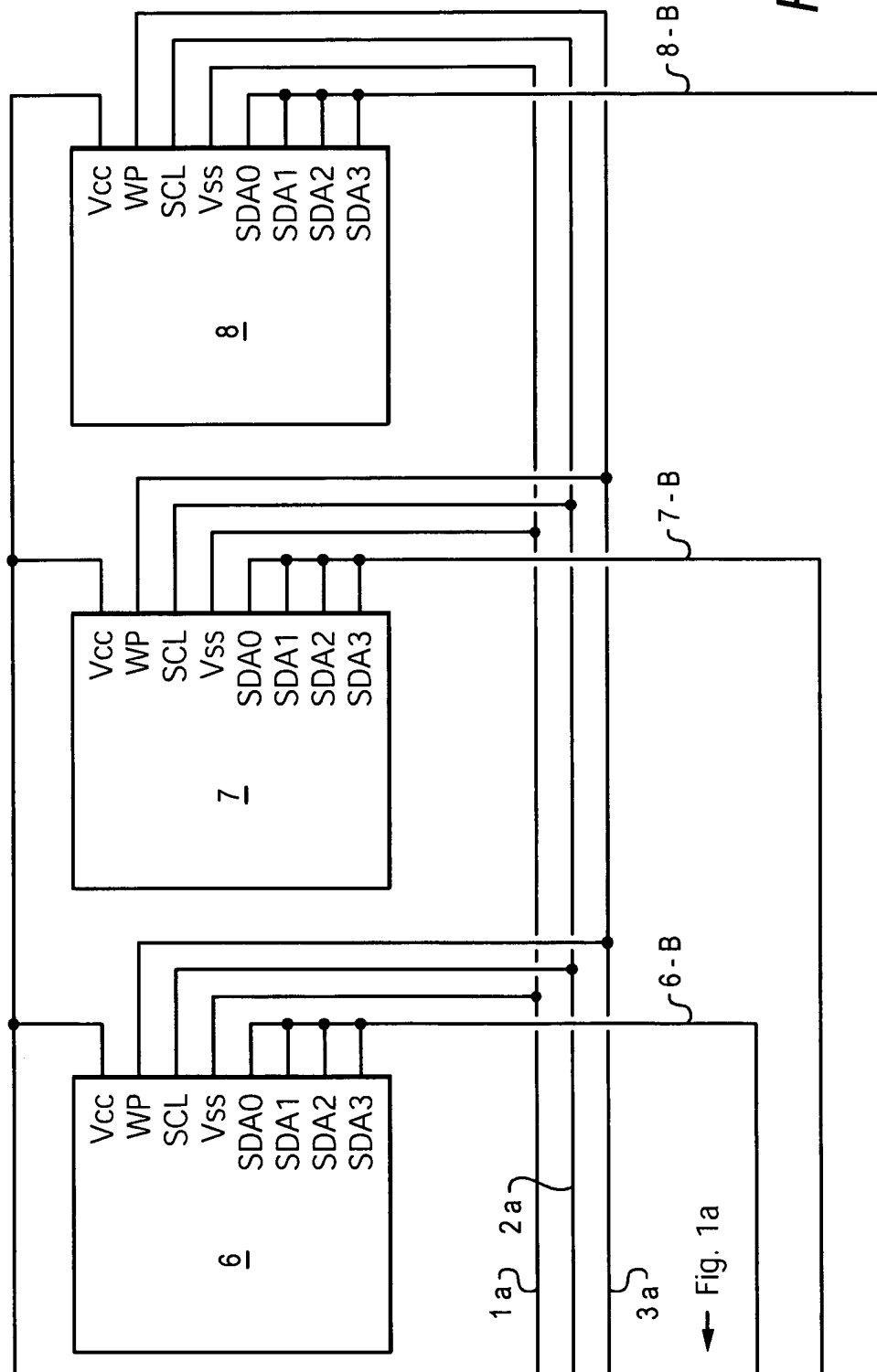
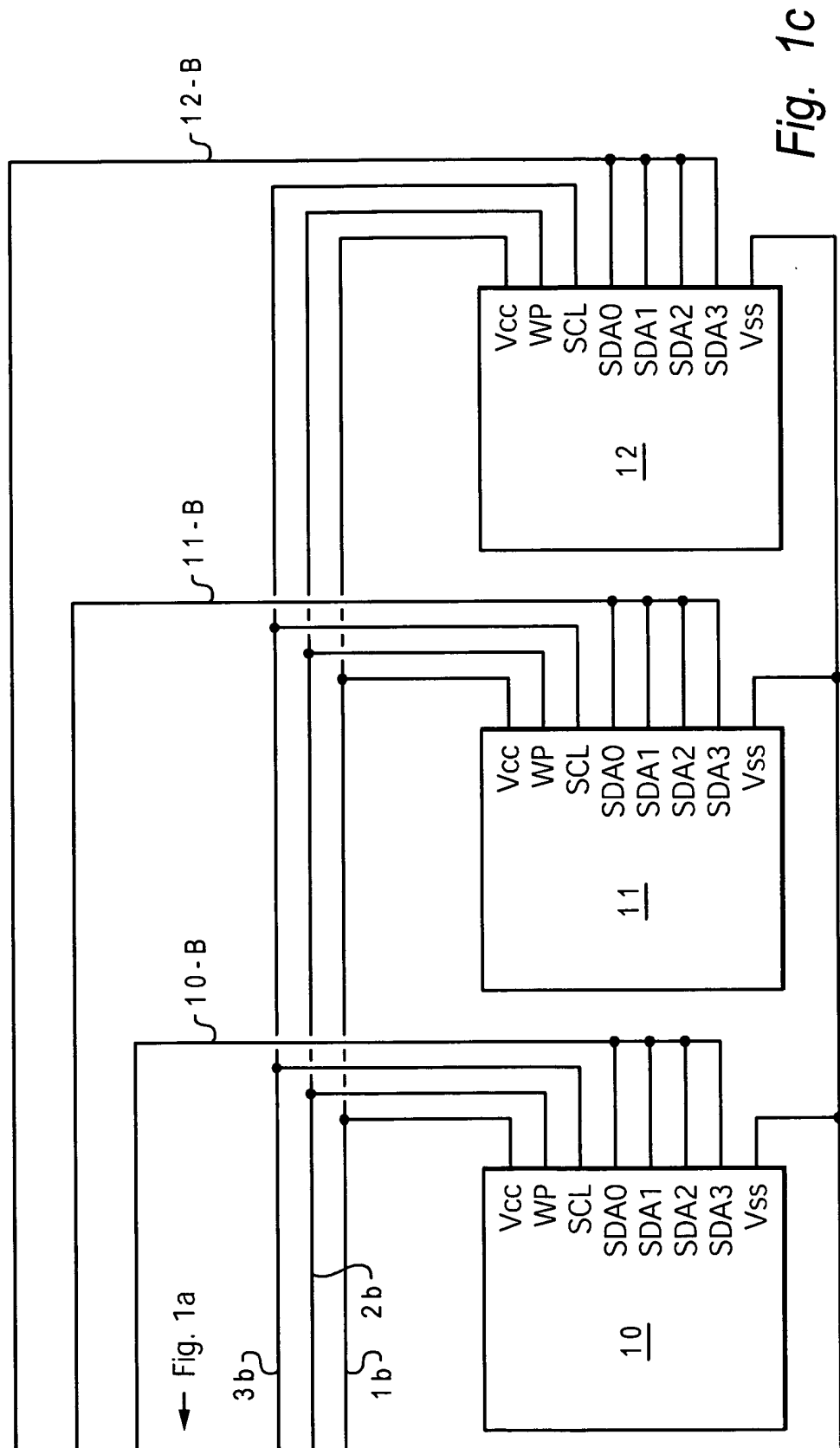


Fig. 1b



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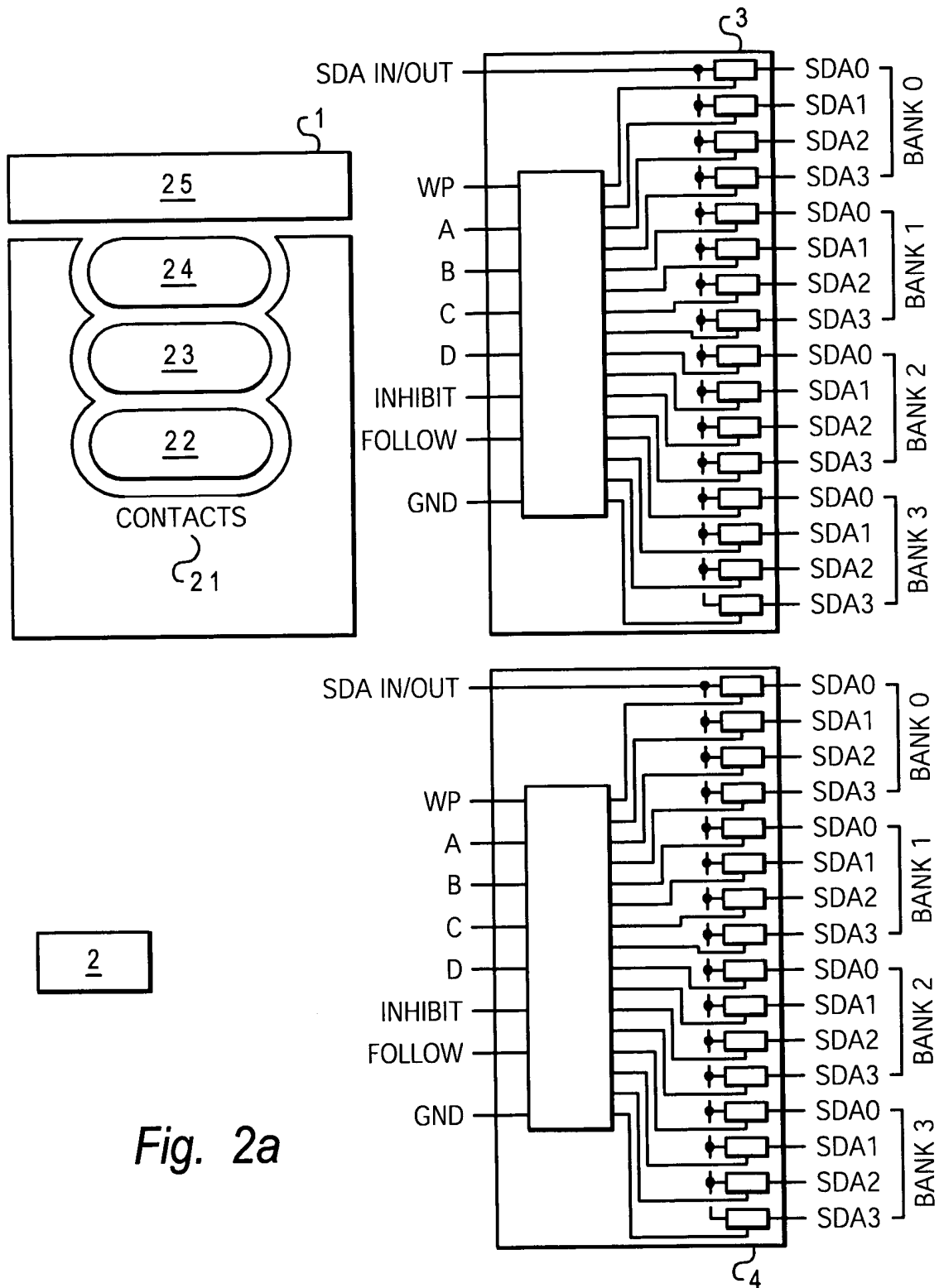
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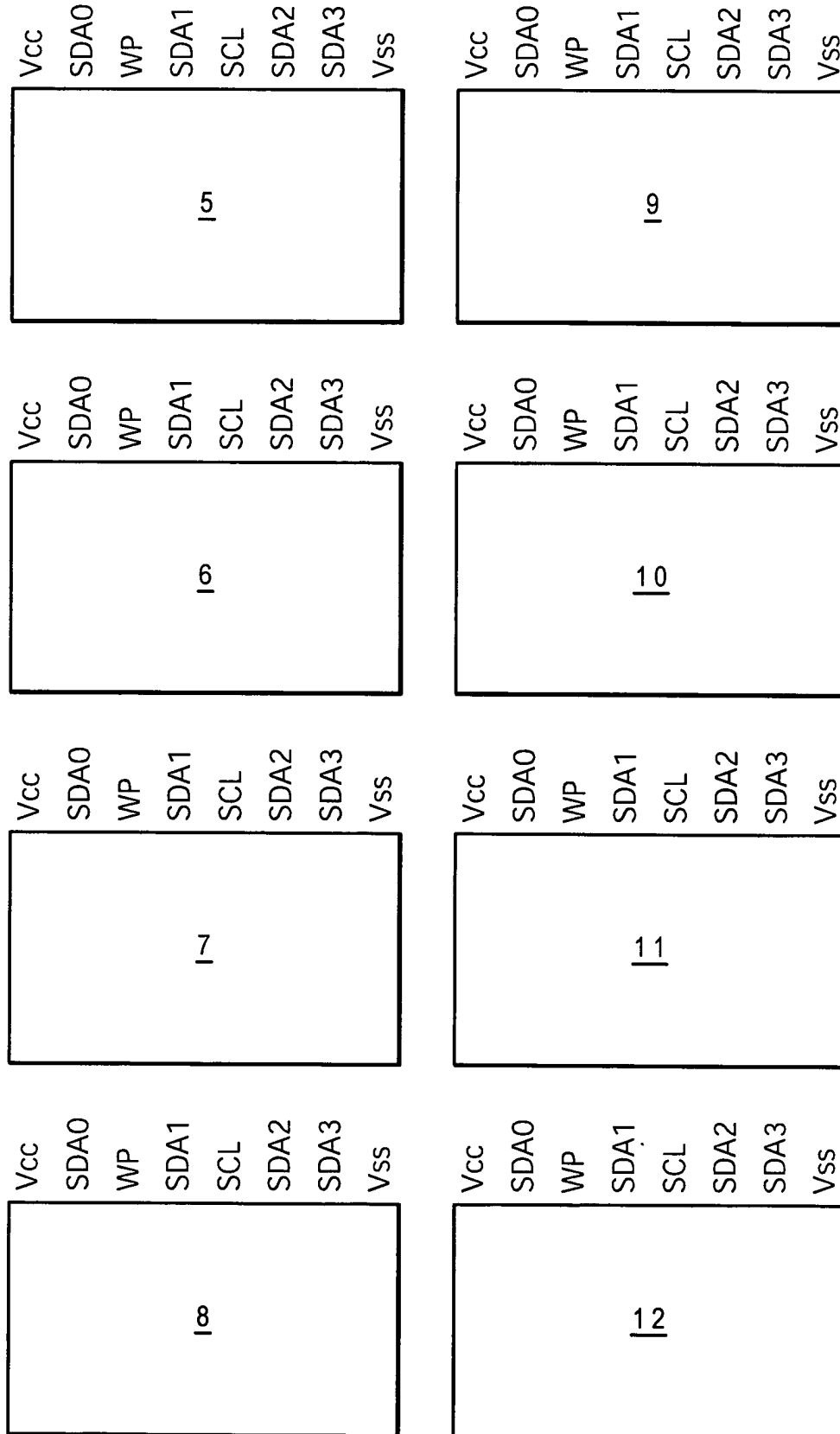


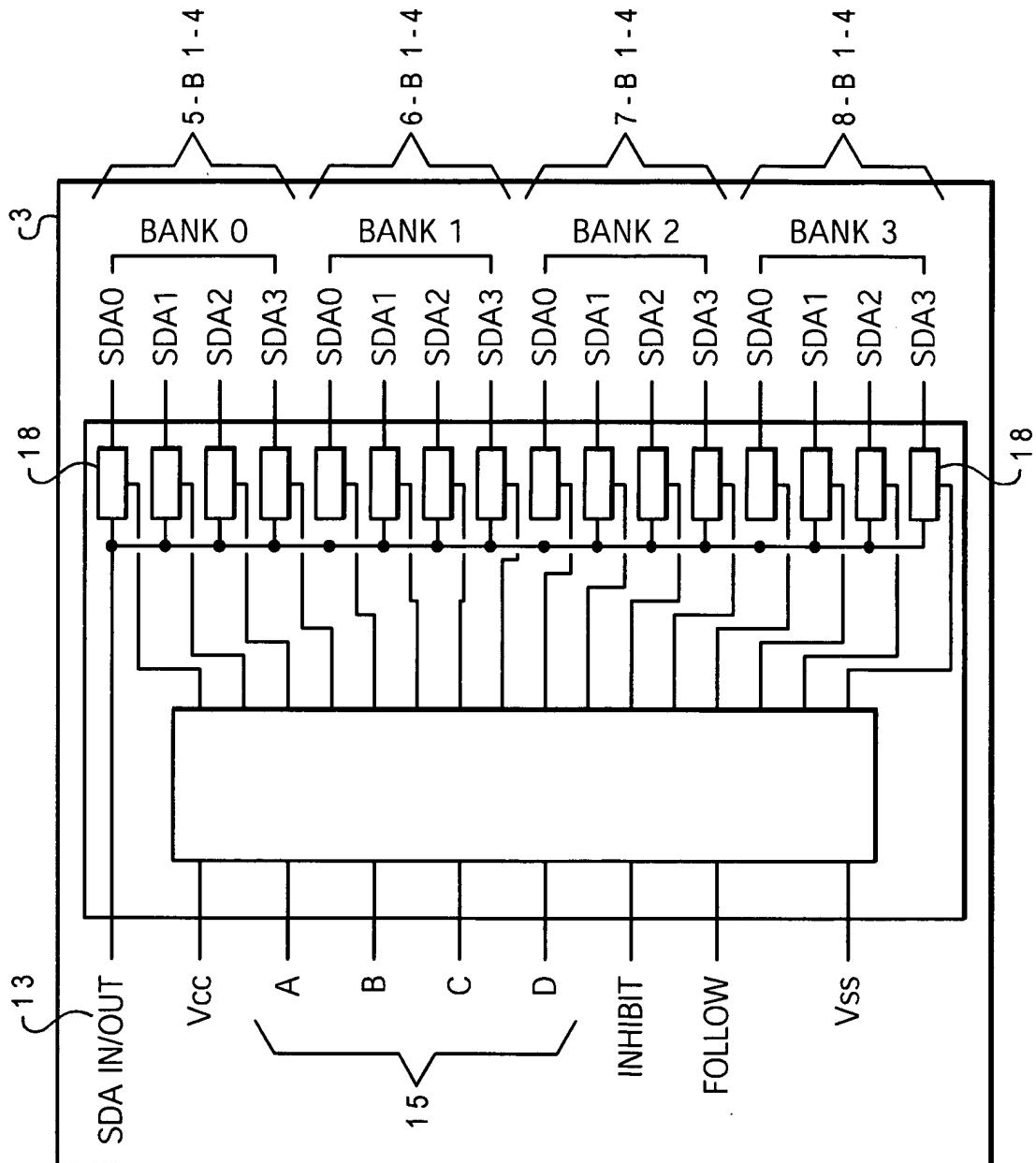


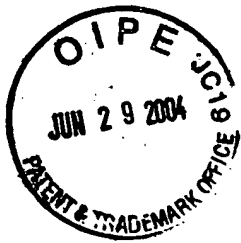
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Fig. 2b







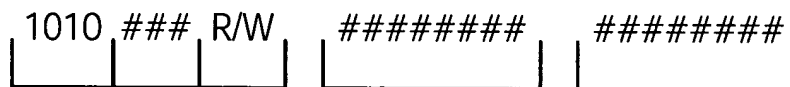
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4 bit parallel address portion defines one of the serial outputs of the dispatcher. Each serial output is connected to one memory unit.

*Fig. 4a*



1010 ### R/W #####

Address low byte for specifying one byte of 64 kbyte EEPROM

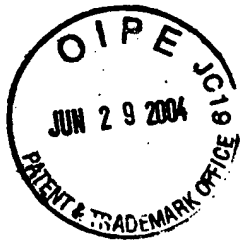
Address high byte for specifying one byte of 64 kbyte EEPROM

Read/write control bit

Three bit code to determine which of the eight 64 kbyte EEPROM memories is addressed

4 bit control nibble which determines any suitable parameter, e.g. a manufacturer's code

*Fig. 4b*



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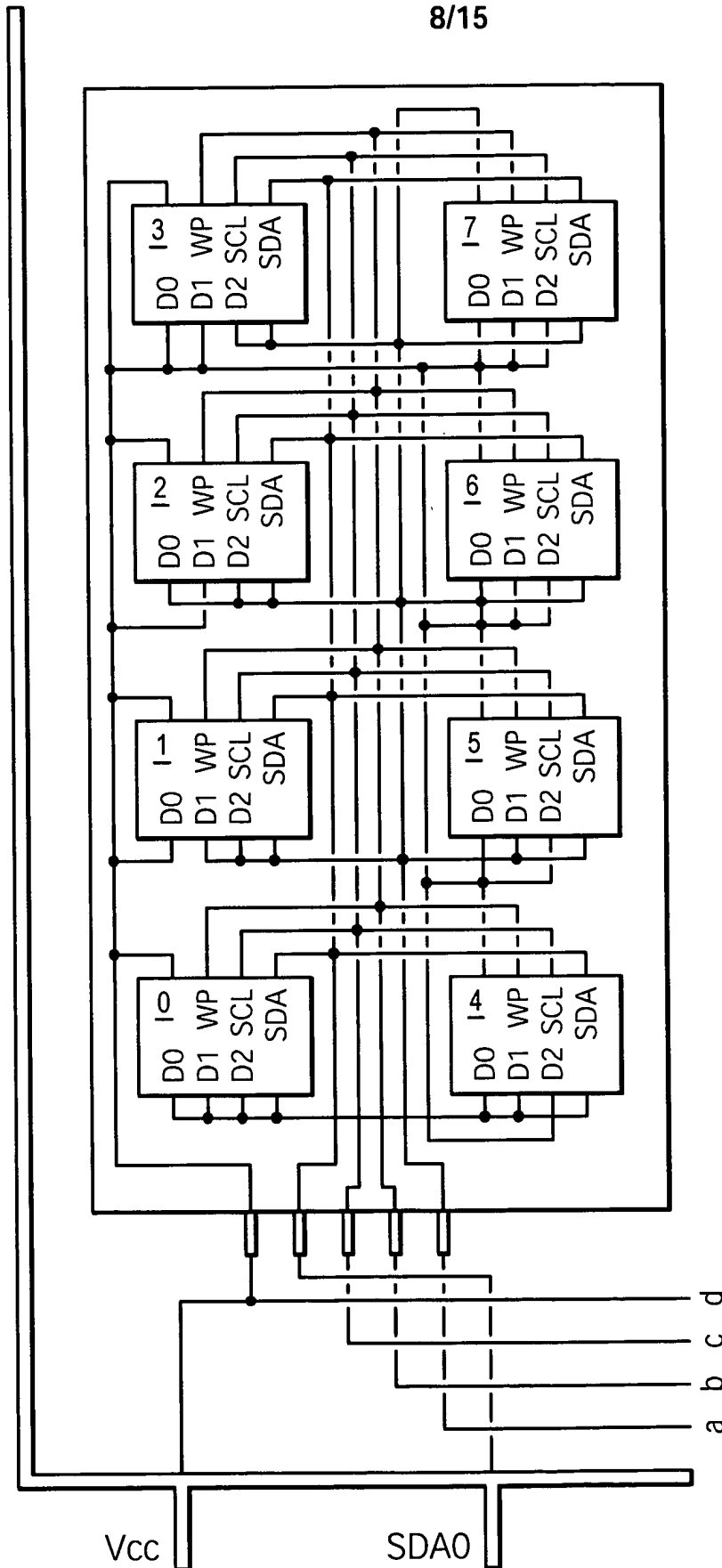


Fig. 5a

→ Fig. 5b



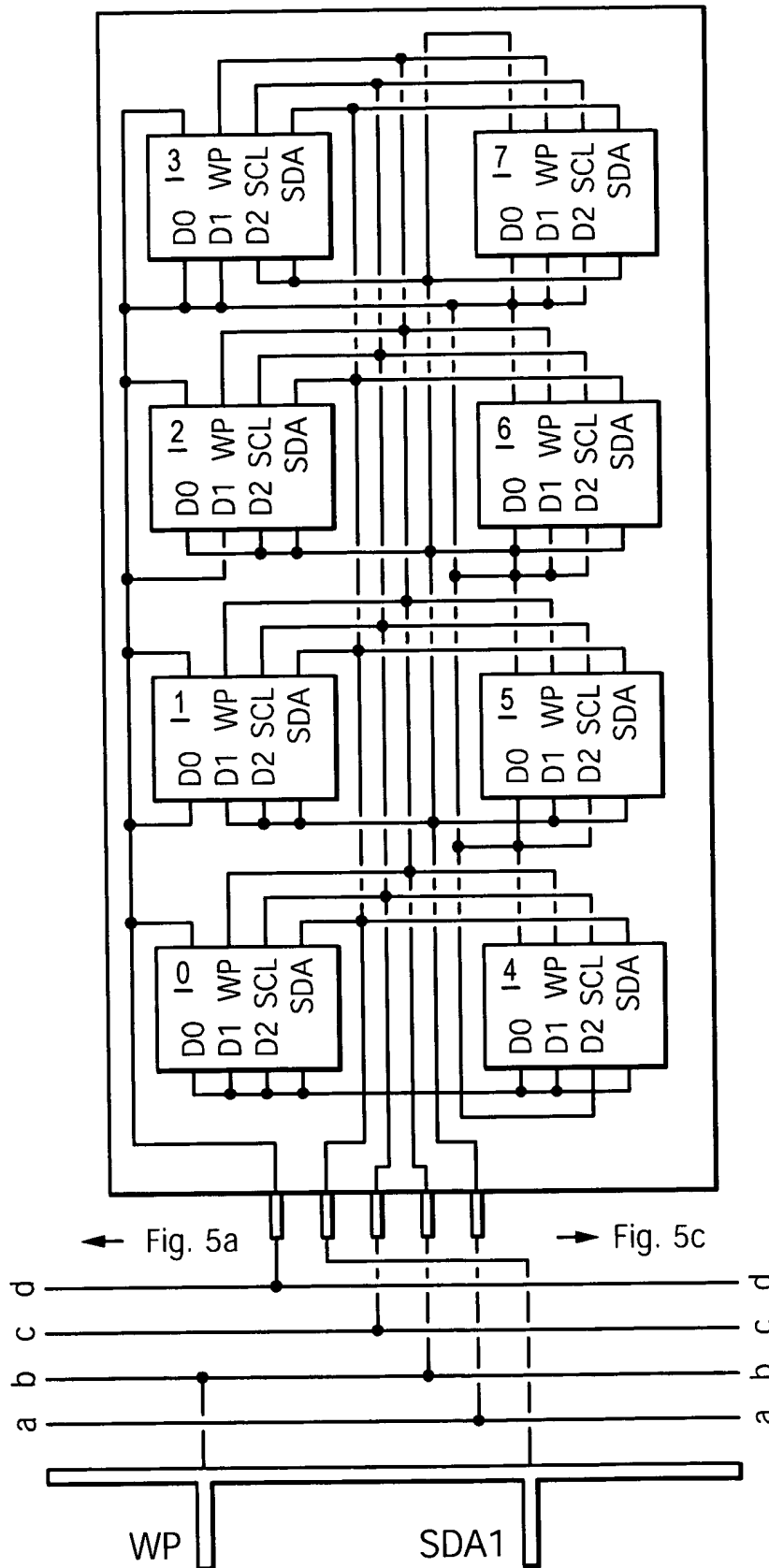


Fig. 5b



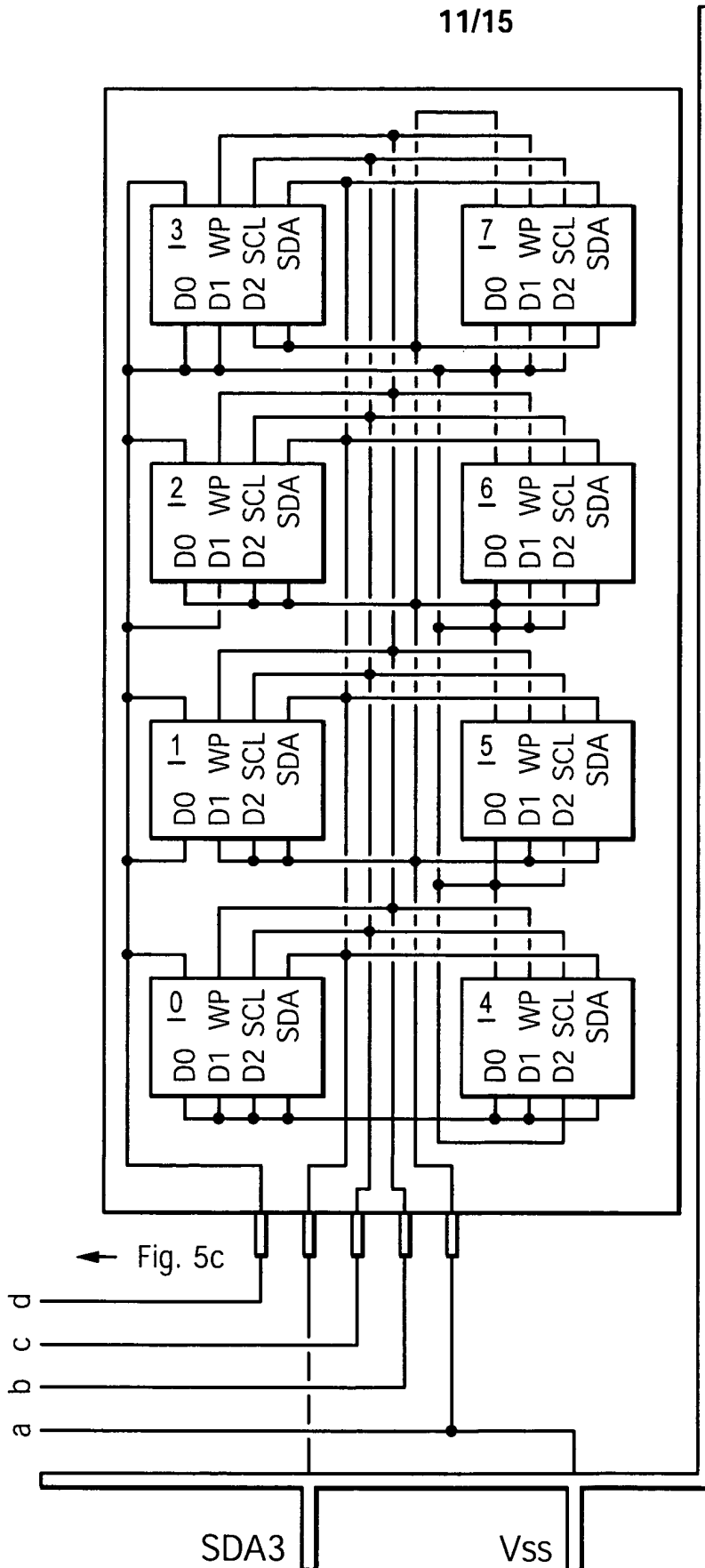


Fig. 5d

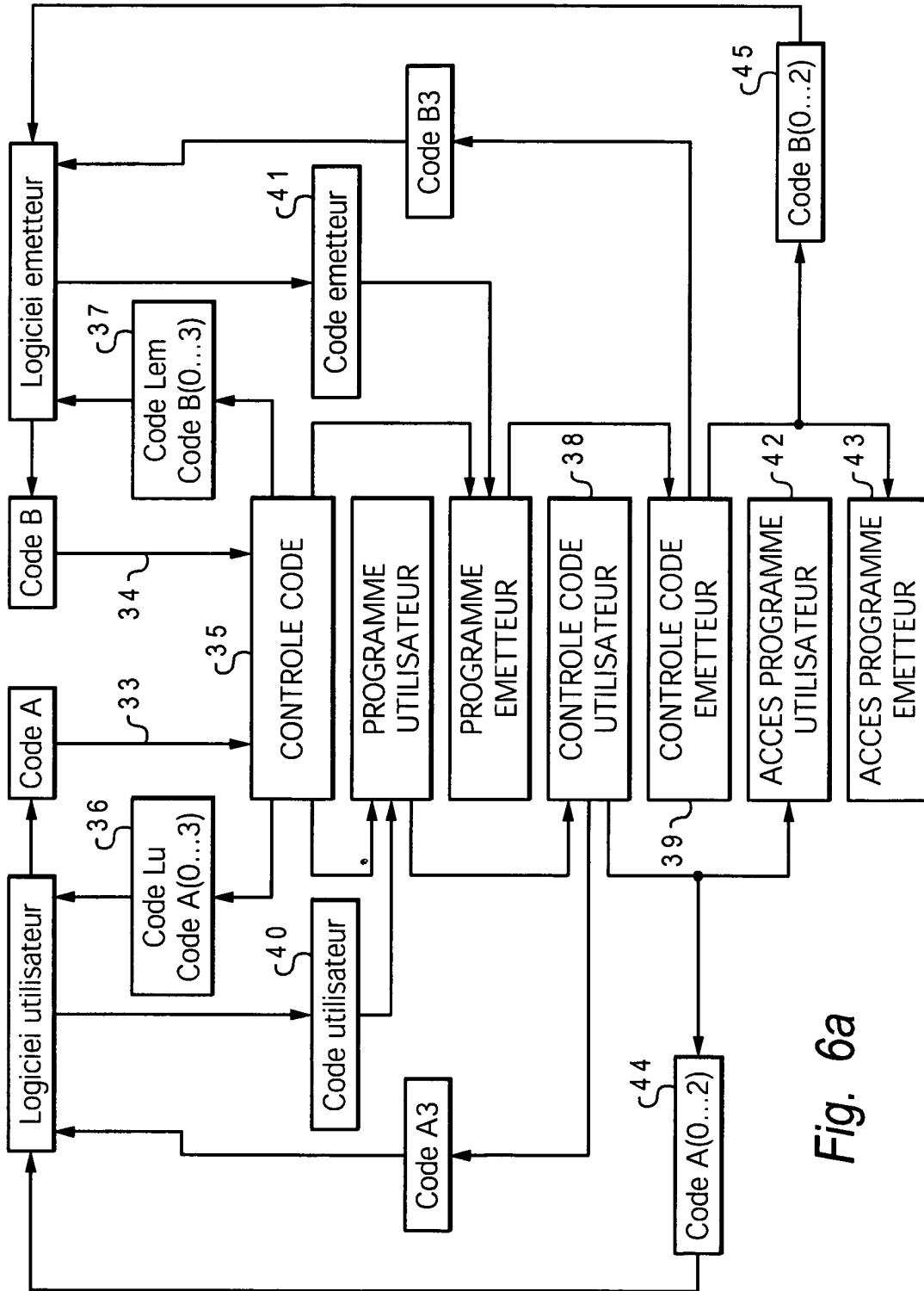
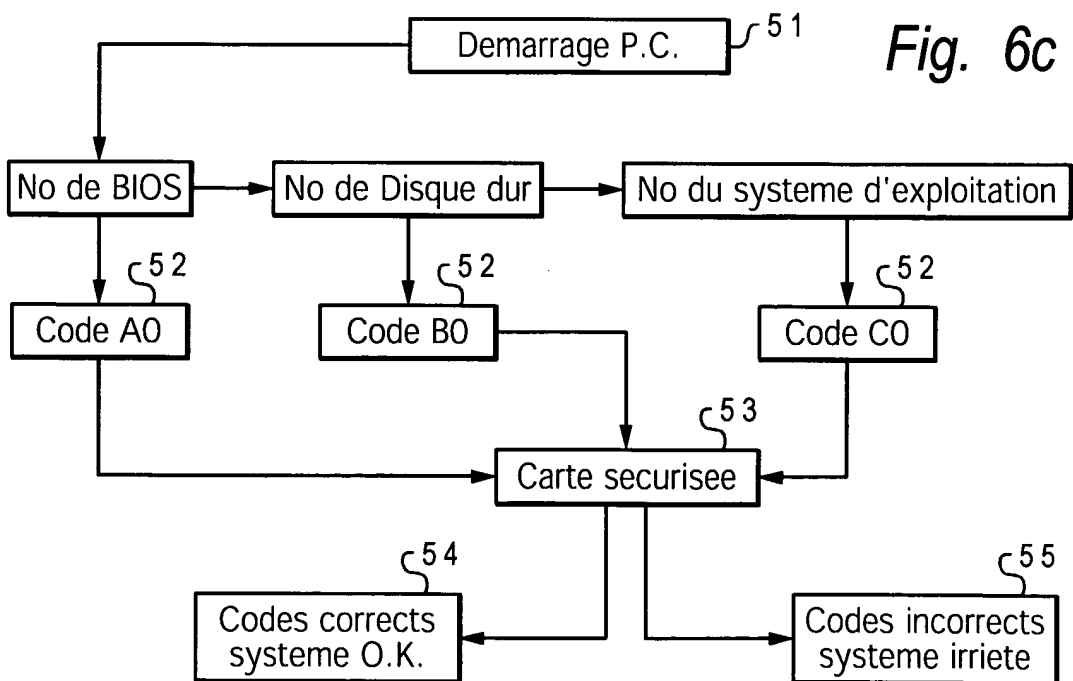
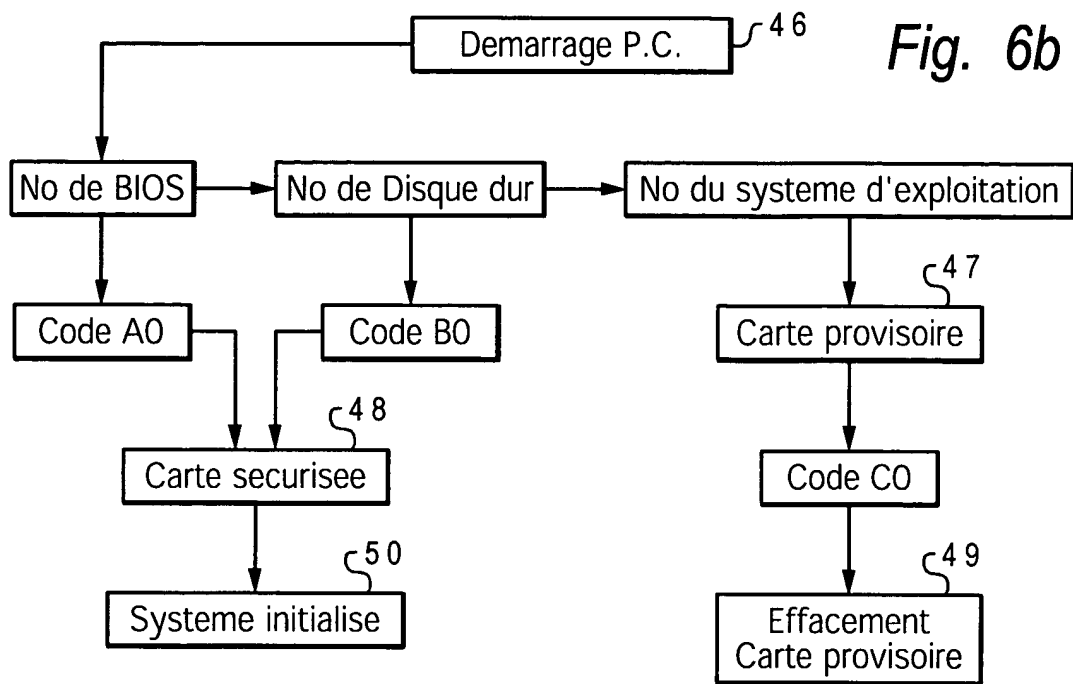


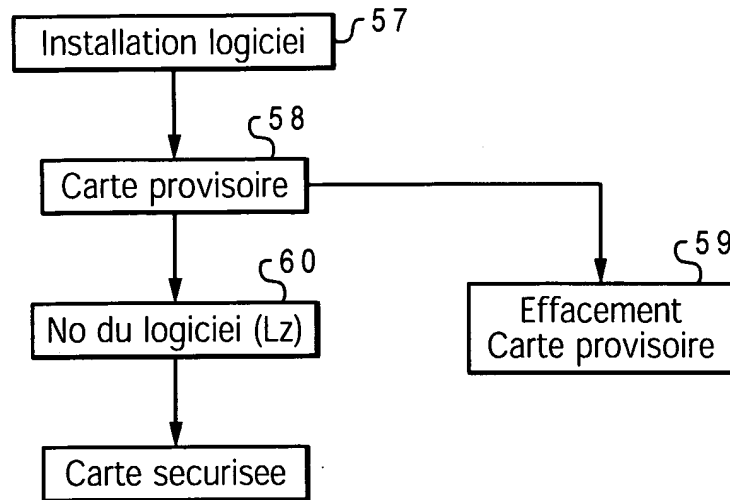
Fig. 6a



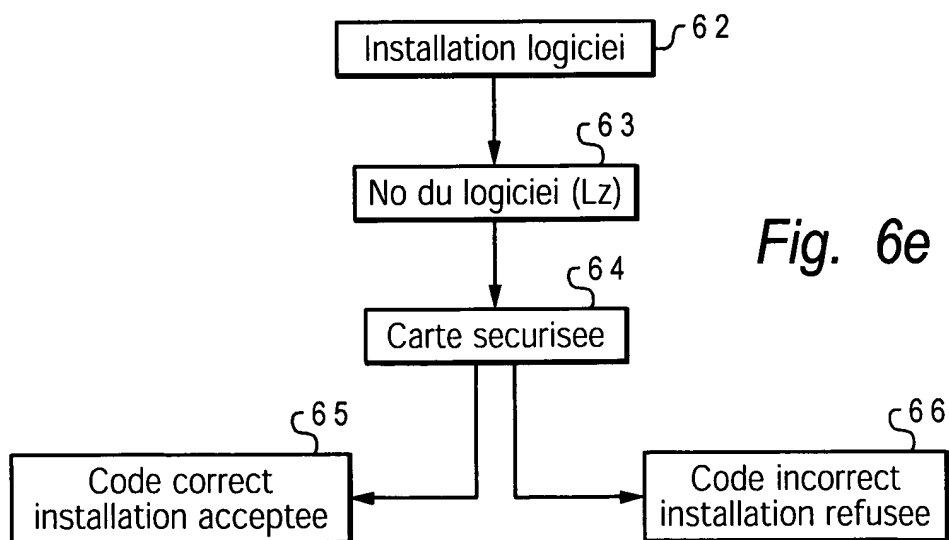


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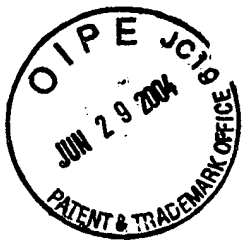
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*Fig. 6d*



*Fig. 6e*



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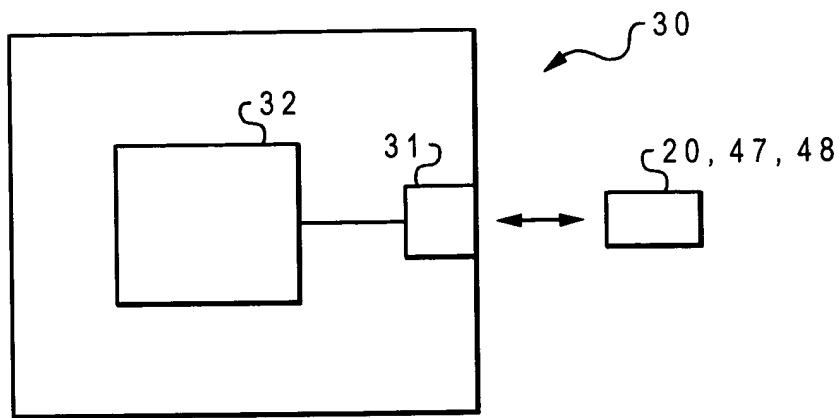


Fig. 7

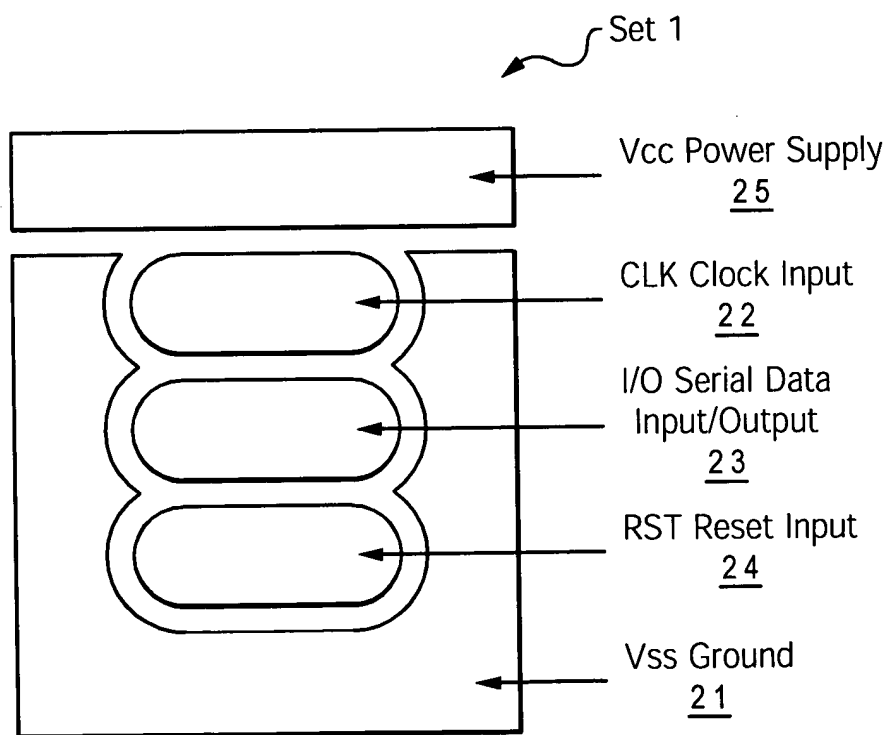


Fig. 8